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D. Remarks

Claim Objections:

Claims 16, 18, 19, and 20 were amended to address these objections.

Claims 16, 18, 19, and 20 were amended to include "first" and "second" processing circuits to clarify the claim.

Rejection of Claims 9, and 14-17 Under 35 U.S.C. §103(a), based on Applicant's Background Art (BACKGROUND ART) in view of *Muramatsu et al.* (JP 59-183455).

The rejection of claims 9 and 14 will first be addressed.

The data processing apparatus of amended claim 9 includes a semiconductor memory circuit that is controlled by control signal inputs to at least one control input. At least one control line is coupled to the at least one control input of the semiconductor memory circuit. A plurality of data processing circuits that share access to the semiconductor memory circuit, each data processing circuit having a control output coupled to the at least one control line. When one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal. Subsequently, when another data processing circuit starts control of the semiconductor memory circuit, the another data processing circuit provides a control signal at its control output at the predetermined potential within the first time period.

As is well understood, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[1]

In this case, the rejection relies on a foreign language document (*Muramatsu)* in support of the rejection. Applicant respectfully requests an English translation of *Muramatsu.*

> "If the document is in a language other than English and the examiner seeks to rely on that document, a translation must be obtained so that the record is clear as to the precise facts the examiner is relying upon in support of the rejection"[2]

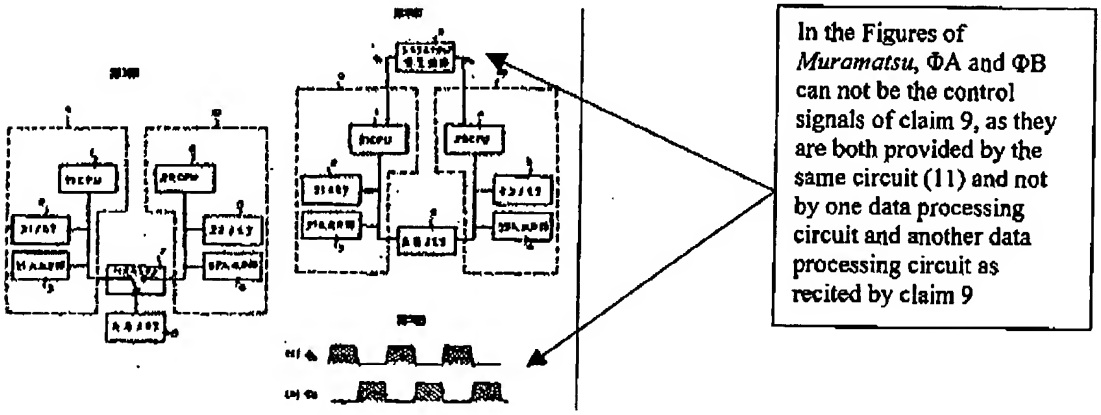
[1] MPEP §2143.
[2] MPEP §706.02(II)

Because the rejection relies on a document in a language other than English and the examiner relies on that document for the rejection, a prima facie case of obviousness cannot be established without an English translation and for this reason the ground for rejection is traversed.

Additionally, or in the alternative, the rejection admits applicant's (BACKGROUND ART) does not show when one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal. Subsequently, when another data processing circuit starts control of the semiconductor memory circuit, the another data processing circuit provides a control signal at its control output at the predetermined potential within the first time period.[3]

Based on the figures published, *Muramatsu* also does not show this limitation.

In *Muramatsu*, the only signals shown are a ΦA and ΦB, which are provided by the same circuit (11) and not by one data processing circuit and another data processing circuit. Thus, ΦA and ΦB can not be the respective control signals of claim 9. There are no other timings of signals disclosed in the figures of *Muramatsu*.



For these reasons, the ground for rejection of claim 9 is traversed.

[3] See last paragraph of page 5 of Final Office Action dated December 19, 2006.

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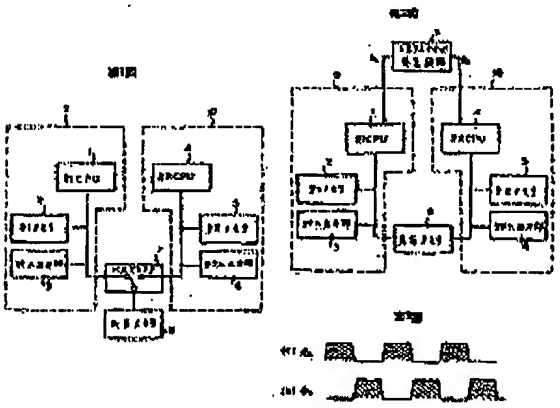
Claim14, which depends from claim 9, is believed to be separately patentable over the cited reference. Claim 14 recites that "at least one control line is directly connected to the control input of the semiconductor memory circuit and the control output of each of the plurality of data processing circuits".

The rejection relies on the *Muramatsu* to show the limitations of claim 14. However, *Muramatsu* does not show or suggest this limitation. None of the lines coming out of CPUs (1 and 4) are shown to be directly connected and therefore there can not be the one control line directly connected to the control input of the semiconductor memory circuit and the control output of each of the plurality of data processing circuits as recited in claim 14.



No lines from CPU (1 and 4) are directly connected with each other and therefore cannot be the control line recited in claim 14.

For these reasons the rejection of claim 14 is traversed.

The rejection of claims 15-17 will now be addressed.

The invention of amended claim 15 is directed to a method of sharing a semiconductor memory circuit with a plurality of data processing circuits. The method includes, when a first data processing circuit ends control of the semiconductor memory circuit, driving first control outputs connected to control lines for the semiconductor memory circuit to predetermined logic values, and subsequently placing the first control outputs in a high impedance state. The method also includes, when a second data processing circuit starts control of the semiconductor memory circuit, second driving control outputs connected to the control lines to the predetermined logic values prior to the first control outputs of the first data processing circuit that is ending control of the semiconductor memory circuit being placed in the high impedance state.

To address this rejection, the arguments set forth with regard to claim 9 are incorporated herein by reference. Namely, the rejection relies on a document in a language other than English

and the examiner relies on that document for the rejection, a prima facie case of obviousness cannot be established without an English translation and for this reason the ground for rejection is traversed.

To further address this rejection, the arguments set forth with regard to claim 14 are incorporated herein by reference. Namely, neither reference shows or suggests the control lines connected to both the first data processing circuit that ends control of the semiconductor memory circuit and the second data processing circuit that starts control of the semiconductor memory circuit. Both references show intervening circuits between the control lines (i.e. the control lines are not connected).

Accordingly, because the cited combination of references is not believed to show or suggest all of the Applicant's claim limitations, this ground for rejection is traversed.

Rejection of Claims 1, 3, 5, and 10 Under 35 U.S.C. §103(a), based on Applicant's Background Art (BACKGROUND ART)) in view of *Muramatsu et al.* (JP 59-183455) further in view of *Wilcox et al.* (USP 6,510,099).

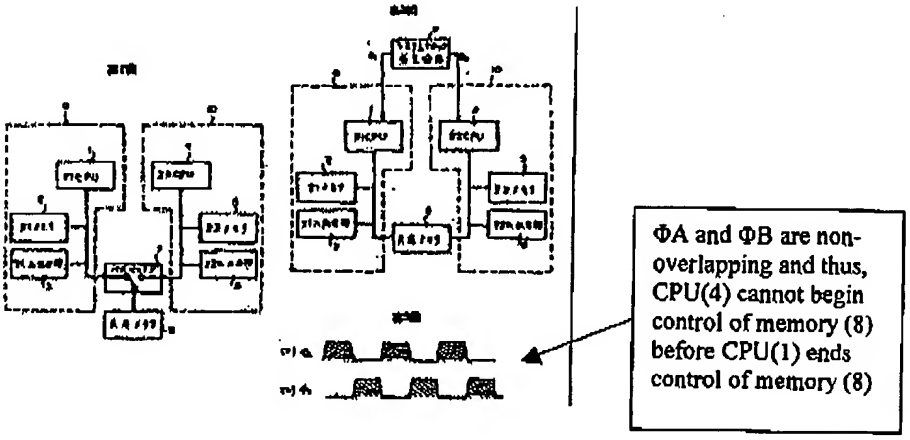
The invention of amended claim 1 is directed to a data processing apparatus that arbitrates sharing of a single semiconductor memory circuit among multiple data processing circuits. The data processing apparatus includes a semiconductor memory circuit and a data processing circuit supplies the semiconductor memory circuit with a first clock enable signal output to the clock enable signal input and a first chip select signal output to the chip select signal input. In the data processing apparatus, before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the first clock enable signal output and first chip select signal input, a different data processing circuit starting control of the semiconductor memory circuit supplies the semiconductor memory circuit with a second clock enable signal output and a second chip enable signal output to the clock enable signal input and chip select signal input. The second clock enable signal output and second chip enable signal output having clock enable signal and chip select signal logic values at the same state as those provided by the data processing circuit ending control of the semiconductor memory circuit.

To address this rejection, the arguments set forth with regard to claim 9 are incorporated herein by reference. Namely, the rejection relies on a document in a language other than English and the examiner relies on that document for the rejection, a prima facie case of obviousness

cannot be established without an English translation and for this reason the ground for rejection is traversed.

The rejection relies on *Muramatsu* to show that before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the first clock enable signal output and first chip select signal input, a different data processing circuit starting control of the semiconductor memory circuit supplies the semiconductor memory circuit with a second clock enable signal output and a second chip enable signal output to the clock enable signal input and chip select signal input.[4] Applicant submits that *Muramatsu* cannot show this element.

Figure 3, of *Muramatsu* shows a timing diagram of two signals ΦA and ΦB. Note, these signals appear to be non-overlapping. Thus, if they are clock signals that enable CPU (1 and 4), respectively, then *Muramatsu* cannot show before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the first clock enable signal output and first chip select signal input, a different data processing circuit starting control of the semiconductor memory circuit supplies the semiconductor memory circuit with a second clock enable signal output and a second chip enable signal output to the clock enable signal input and chip select signal input as recited in claim 1.



For all of these reasons, the combination of references is not believed to show or suggest all the limitations of claim 1, and this ground for rejection are traversed.

The rejection of claim 10 will now be addressed.

[4] See 2nd paragraph of page 8 of Final Office Action dated 12/19/2006.

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Maramatsu.*, Applicant incorporates by reference herein the same general comments set forth above for independent claim 9.

Rejection of Claims 18-20 Under 35 U.S.C. §103, based on Applicant's Background Art in view of *Muramatsu.*, and further in view of *Askinazi et al.* (USP 4,453,21).

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Muramatsu*, Applicant incorporates by reference herein the comments set forth above for independent claim 15.

Claims 16, 18, 19, and 20 have been amended not in response to the cited art, but to clarify elements of the invention. No new matter has been added. The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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